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| 09/654,845 | 09/01/2000 | Jifa Hao | 87552.99R272/SE-1528PD | 6844 |

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THOMAS R. FITZGERALD, ESQ.
16 E. MAIN STREET, SUTIE 210
ROCHESTER, NY 14614-1803

| EXAMINER | |
|---|---|
| NADAV, ORI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/654,845 | HAO ET AL. | |
| | Examiner | Art Unit | |
| | Ori Nadav | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8,10-15,17 and 35-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-15,17 and 35-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

Claims 39-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 35 recites a third boundary between the N+ doped region and the P-well or the N-doped layer. There is no support in the specification for a device which meets both limitations of claim 1 (a third boundary between the N+ doped region and the P-well or the N-doped layer) and the limitations of the N+ doped region is separated from the P-doped well by the N-doped layer, the N+ doped region is within the P-doped well, and the N+ doped region abuts the P+ doped region, as recited in claims 39-41.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claim 35-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of a second boundary being more shallow than the first or third boundaries, as recited in claim 36, is unclear as to which part of the first, second and third boundaries applicant refers, since each of the first, second and third boundaries are located at various heights.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1-8, 10-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choy (5,171,705) in view of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858).

Regarding claims 1 and 35, Choy teaches in figure 4 and related text a power semiconductor device comprising: a semiconductor substrate with two surfaces and an N+ doped layer 3 extending into the substrate from one surface thereof, an N- doped layer 5 over the N+ doped layer, a P- doped well 7 formed in the N- doped layer and extending from the other surface of the substrate into the N- doped layer, a P+ doped region 10 formed in the P- doped well and also extending from the other surface of the substrate into the P doped well,

an N+ doped region 9 (the N+ region which is located away from the P doped well) formed in the other surface of the substrate and in the N- doped layer (the N+ doped region is formed in a P doped well, and the P doped well is formed in the N- doped layer. Therefore, the N+ doped region is formed in the N- doped layer), said N+ doped region laterally spaced from the P+ doped region and the P doped well.

Choy does not teach the thickness of the P+ doped region and the P doped well, and recombination centers comprising noble metal impurities disposed substantially in the N - doped layer and P doped well.

Regarding the claimed limitations of P- doped and P+ doped layers having a combined thickness of about 5 microns to about 12 microns, Schlangenotto et al. (5,063,428) teach that the P- doped 2a and P+ doped 2b layers have a doping curve similar to that of figure 4 (column 7, lines 3-5). Schlangenotto et al. (5,063,428) further teach P+ doped layer 2b having a thickness of 0.2 microns (column 5, lines 33-35), wherein P- doped layer 2a should have a thickness greater than 5 microns and less than 70 microns (column 5, line 65 to column 6, line 3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use P- doped 2a and P+ doped 2b layers having a combined thickness of about 5 microns to about 12 microns, in Choy's device, in order to form a device as small as possible within the criteria limits of Schlangenotto et al. (5,063,428), without compromising the characteristics of the device. Note that at the time the claimed invention was made the size of semiconductor devices has been dramatically minimized.

Regarding the claimed limitations of forming recombination centers comprising noble metal impurities disposed substantially in the N - doped and P- doped layers, Schlangenotto et al. (5,063,428) teach that it is known in the art to form recombination centers comprising noble metal impurities in power diodes in order to reduce charge carrier life (column 1, lines 24-29). Schlangenotto et al. (5,063,428) further teach forming recombination centers in the power diode of figure 3 in order to improve the characteristics of the device (column 5, lines 39-46).

Schlangenotto et al. (5,773,858) teach that it is known to form recombination centers in high speed power diodes in order to improve the dynamic characteristics by lowering the charge carrier life (column 1, lines 21-25).

Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) do not limit the location of the recombination centers to specific areas of the power diodes. Therefore, it is understood to an artisan that the recombination centers are formed throughout the power diodes.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form recombination centers comprising noble metal impurities in Choy's device, in order to order to improve the dynamic characteristics of the device by lowering the charge carrier life by a well known method. The combination is motivated by the teachings of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) who point out the advantages of forming recombination centers in power diodes. Note that the broad recitation of the claim does not require the recombination centers to be located only in the N - doped and P- doped layers.

Regarding claims 2 and 3, Choy does not teach a P- doped well having a thickness of about 4 microns to about 10 microns and P+ doped region having a thickness of about 0.1 to about 2 microns. Schlangenotto et al. (5,063,428) teach P+ doped layer 2b having a thickness of about 0.1 to about 2 microns (column 5, lines 33-35). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use P- doped well having a thickness of about 4 microns to about 10 microns and P+ doped region having a thickness of about 0.1 to about 2 microns in the device of Choy, in order to form a device as small as possible within the criteria design limits.

Regarding claims 4-7, Choy does not teach a P- doped well has a dopant level of at least 10E16 atoms/cm3 and a dopant level of about 2.5x 10E17 atoms/cm3 and a P+ doped region having a dopant level of about 6x10E19 atoms/cm3, respectively. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a P- doped well having a dopant level of about 2.5x 10E17 atoms/cm3 and a P+ doped region having a dopant level of about 6x10E19 atoms/cm3 in prior art's device, since forming a P- doped well having a dopant level of about 2.5x 10E17 atoms/cm3 is within the skills of an artisan, subject to routine experimentation and optimization. Note that differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ

233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 8, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an N- doped layer having a dopant level of about 10E14 atoms/cm3 to about 10E15 atoms/cm3 in prior art's device since forming an N -doped layer having a dopant level of about 10E14 atoms/cm3 to about 10E15 atoms/cm3 is within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 10-11, Schlangenotto et al. (5,063,428) teach noble metal impurities comprise platinum (column 1, lines 26-27).

Regarding the process limitations recited in claim 12 ("recombination centers are formed by platinum diffusion through the N + doped substrate"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180

USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in □product by process□ claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 13-14, prior art does not teach platinum impurities at a concentration of about 1x10E15 to about 1x10E16 atoms/cm3, and about 2x1015 atoms/cm3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form platinum impurities at a concentration of about 1x10E15 to about 1x10E16 atoms/cm3, and about 2x1015 atoms/cm3 in prior art's device, in order to adjust the device characteristics according to the requirements of the application in hand, since the reverse current and the device performance depend on the platinum impurities concentration.

Regarding claims 15 and 17, Choy teaches in figure 4 a device comprising a diode, a MOSFET or an IGBT power device, wherein an N+ doped region disposed in an N - doped layer.

Claims 35-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Temple (4,809,047) in view of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858).

Temple teaches in figure 8 and related text a power semiconductor device comprising: a semiconductor substrate with two surfaces and an N+ doped layer 62 extending into the substrate from one surface thereof, an N- doped layer 64 over the N+ doped layer, a P- doped well 68 formed in the N- doped layer and extending from the other surface of the substrate into the N- doped layer, a P+ doped region 72 formed in the P- doped well and also extending from the other surface of the substrate into the P doped well,

A P- layer 68 having a first thickness and forming a first boundary with the N- doped layer 64, a P+ doped region 72 formed in the P- doped well and extending from the other surface of the substrate into the P-doped well to have a second thickness and to form a second boundary between the P+ doped region and the P- doped well, an N+ doped region formed in the other surface of the substrate, said N+ doped region having a third thickness and forming a third boundary between the N+ doped region and the P- well or the N-doped layer,

wherein the P+ doped region is vertically thinner than the P- doped well and vertically thinner than the N+ doped region.

Temple does not teach recombination centers comprising noble metal impurities disposed substantially in the N - doped layer and P doped well.

Regarding the claimed limitations of forming recombination centers comprising noble metal impurities disposed substantially in the N - doped and P- doped layers,

Schlangenotto et al. (5,063,428) teach that it is known in the art to form recombination centers comprising noble metal impurities in power diodes in order to reduce charge carrier life (column 1, lines 24-29). Schlangenotto et al. (5,063,428) further teach forming recombination centers in the power diode of figure 3 in order to improve the characteristics of the device (column 5, lines 39-46).

Schlangenotto et al. (5,773,858) teach that it is known to form recombination centers in high speed power diodes in order to improve the dynamic characteristics by lowering the charge carrier life (column 1, lines 21-25).

Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) do not limit the location of the recombination centers to specific areas of the power diodes. Therefore, it is understood to an artisan that the recombination centers are formed throughout the power diodes.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form recombination centers comprising noble metal impurities in Temple's device, in order to order to improve the dynamic characteristics of the device by lowering the charge carrier life by a well known method. The combination is motivated by the teachings of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) who point out the advantages of forming recombination centers in power diodes. Note that the broad recitation of the claim does not require the recombination centers to be located only in the N - doped and P- doped layers.

Regarding claims 36 and 39-41, Temple teaches in figure 8, a second boundary being more shallow than the first or third boundaries, wherein the N+ doped region is separated from the P-doped well by the N-doped layer, wherein the N+ doped region is within the P-doped well, and wherein the N+ doped region abuts the P+ doped region.

Regarding claims 37-38, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the ratio of thickness of the P+ doped region to the P-doped well between 1:40 and 1:5, wherein the P+ doped region is between 0.1 to 2.0 microns thick and the P-doped well is between 4.0 and 10.0 microns thick, in Temple's device, in order to form a device as small as possible within the criteria limits of Schlangenotto et al. (5,063,428), without compromising the characteristics of the device. Note that at the time the claimed invention was made the size of semiconductor devices has been dramatically minimized.

***Response to Arguments***

Applicant argues that there is support for a device which meets both limitations of claim 1 (a third boundary between the N+ doped region and the P-well or the N-doped layer) and the limitations of the N+ doped region is separated from the P-doped well by the N-doped layer, the N+ doped region is within the P-doped well, and the N+ doped region abuts the P+ doped region, as recited in claims 39-41, because there is no requirement for a dependent claim to read on both species of the generic claim 35.

The examiner agrees that there is no requirement for a dependent claim to read on both species of a generic claim. However, in this case, Claim 35 recites a third boundary between the N+ doped region and the P-well or the N-doped layer. Both conditions must be met. When dependent claims 39-41 are introduced, both conditions can not be met since each of the dependent claims recites specific limitation, which is contradictory to the requirement of the third boundary, as recited in claim 35. For example, claim 39 recites "N+ doped region is separated from the P-doped well by the N-doped layer". This condition is contradictory to the requirement of claim 35, wherein a third boundary must also exist between the N+ doped region and the P-well.

Applicant argues that Choy does not teach an N+ doped region laterally spaced from the P+ doped region and the P doped well.

Figure 4 of Choy depicts four N+ doped regions 9. The N+ doped region 9 located on the right side of the figure is clearly away from the P doped well located on the left side of the figure. Therefore, Choy teaches an N+ doped region laterally spaced from the P+ doped region and the P doped well, as claimed.

Applicant argues that Choy does not meet the limitation of claim 15 that provides for a P+ doped region in the other (top) surface that is shallower than the N+ doped region in that surface.

Claim 15 does not recite a P+ doped region in the other (top) surface that is shallower than the N+ doped region in that surface. Claim 15 recites an N+ doped region disposed in an N -doped layer.

Applicant argues that Schlangenotto et al. do not limit the location of recombination centers to specific areas of the power diode, and since claim 1 calls for a structure with minimal to no recombination centers in the N+ regions, Schlangenotto et al. do not teach the claimed limitations.

Claim 1 does not recite a structure with minimal to no recombination centers in the N+ regions. Therefore, prior art teaches the claimed limitations.

Applicant argues that Shlangenotto does not teach recombination centers disposed substantially in the N- doped layer and P- doped well, because Shlangenotto does not limit the location of the recombination centers, and claim 1 does not recite forming recombination centers throughout the diode.

The broad recitation of claim 1 does not preclude the recombination centers from being present in areas other than the N- doped layer and P- doped well. Therefore, since Shlangenotto teaches forming recombination centers throughout the diode, these recombination centers would be also present in the N- doped layer and P- doped well, as claimed.

Applicant argues that the final rejection is improper, because it fails to consider evidence of criticality that is present in the specification.

The examiner did not find evidence of criticality in the specification. The specification recites an improvement in avalanche capability over prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
3/15/06

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800